Influence of the Gate Recess on the Performance of Enhancement-Mode AlGaN/GaN HEMTs

Stanislav Vitanov and Vassil Palankovski

Abstract - **After the excellent performance achieved by normally-on AlGaN/GaN high electron mobility transistors (HEMTs), research focus has shifted to normally-off structures. We explore the advantages offered by the recessed-gate technique using our two-dimensional device/circuit simulator Minimos-NT. Excellent agreement with experimental data is achieved, and theoretical AC performance for different recess-depths is studied.**

Keywords – **device simulation, normally-off HEMTs, GaN**

I. INTRODUCTION

The properties of GaN and AlN and their heterostructures have encouraged the research of AlGaN/GaN based transistors for various applications in the last decade. Consequently, outstanding results have been reported for the depletion mode (D-mode) high electron mobility transistors. However, for several applications enhancement mode (E-mode) devices are essential. In analog electronics they supersede the negative voltage supply and also assure a safe state in case of power loss. In digital electronics, they allow complementary FET-based logic [1]. Normally-off operation is also a requirement for automotive applications (e.g. hybrid vehicles) [2]. Despite the interest in E-mode operation, the excellent results as in D-mode devices remain to be seen.

The first E-mode GaN transistor, reported back in 1996 by Khan et al. [3], was achieved by using thinner AlGaN barriers. However the main issue with recess techniques is the damage introduced in the barrier. Recent developments include several annealing steps [4] and fluoride-based plasma treatment [5]. Several approaches relying on additional layers introduced under the gate have been also proposed. Hu et al. [6], suggested a pn-junction under the gate. Mizutani et al. [7] proposed an InGaN cap layer in order to raise the conduction band under the gate. Also Higashiwaki et al. [8] reported an AlN/GaN structure with thin AlN layer, with positive threshold voltage.

In this work, we analyze the trade-off between high frequency performance and threshold voltage achieved by gate recess technique [9]. Results from two-dimensional hydrodynamic simulations, supported by experimental data [10], are presented.

S. Vitanov and V. Palankovski are with the Advanced Materials and Device Analysis Group, Institute for Microelectronics, TU Vienna, Gusshausstrasse 27–29, 1040 Vienna, Austria, e-mail: vitanov@iue.tuwien.ac.at, palankovski@iue.tuwien.ac.at

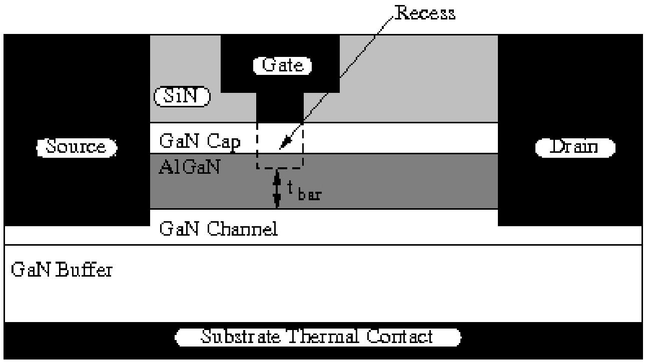

Figure 1. Schematic layer structure of the investigated device

II. DEVICE STRUCTURE

AlGaN/GaN depletion mode (DHEMTs) and enhancement mode (EHEMTs) HEMT structures with T-gates of 250 nm length share the same layer specification and are processed on the same SiC wafer. The devices consist of GaN buffer, 22 nm thick $Al_{0.22}Ga_{0.78}N$ ($Al_{0.18}GaN_{0.82}N$ for the EHEMT device) barrier layer, 3 nm thick GaN cap layer, and SiN passivation (Fig. 1). The cap and part of the barrier layer under the gate of the EHEMT are recessed by Cl_2 plasma etching. A remaining AlGaN barrier thickness t_{bar}=11 nm is assumed. The Ohmic contacts are assumed to reach the two-dimensional electron gas in the channel.

III. SIMULATION SETUP

The devices are analyzed by means of two-dimensional hydrodynamic simulations using Minimos-NT, which was successfully employed for the development of new generation of AlGaN/GaN HEMTs [11], [12]. Material properties, such as band energies, carrier mobilities, and carrier relaxation times are properly modeled. The densities of the polarization charges at the channel/barrier interface and at the barrier/cap interface are determined by calibration against the experimental data to be 9×10^{12} cm^{-2} and -2×10^{12} cm^{-2}, respectively. Low Ohmic contact resistances of 0.2 Ωmm are considered [10].

Self-heating effects are accounted for by using substrate thermal contact resistance of R_{th}=5 K/W. This value lumps the thermal resistance of the nucleation layer and the substrate. The impact of thermionic emission and field emission effects, which determine the transport across the heterojunctions is assessed.

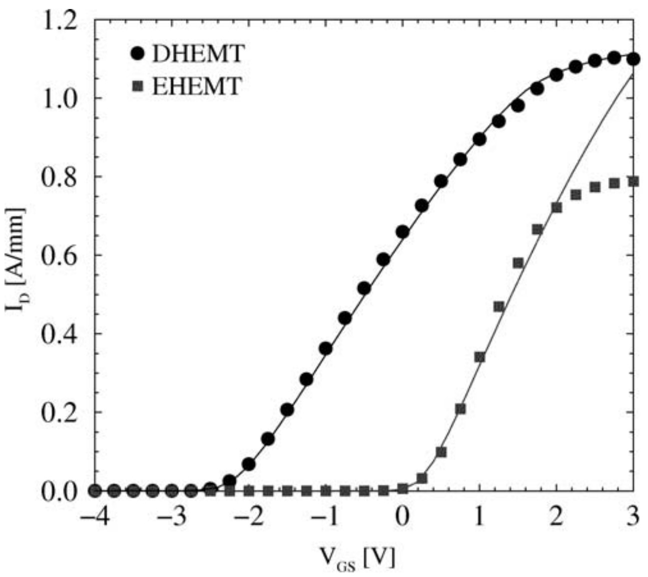

Figure 2. Transfer characteristics at V_{DS}=7 V: lines – simulation, symbols – experimental data

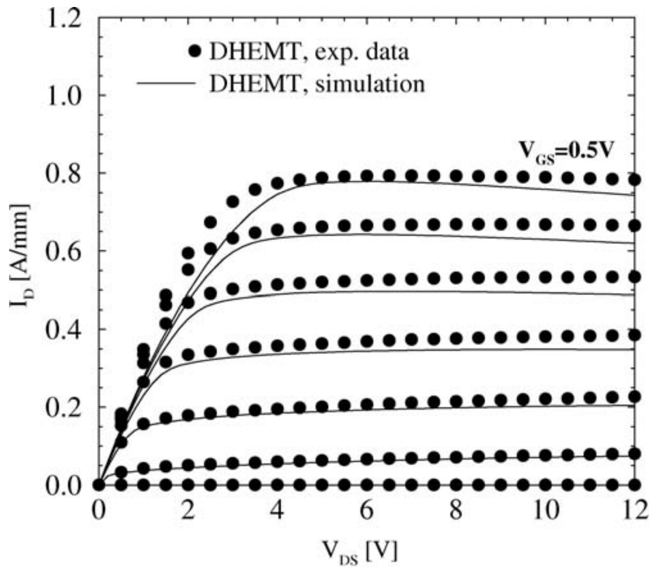

Figure 4. Comparison of the output characteristics (DHEMT), V_{GS} stepping 0.5 V

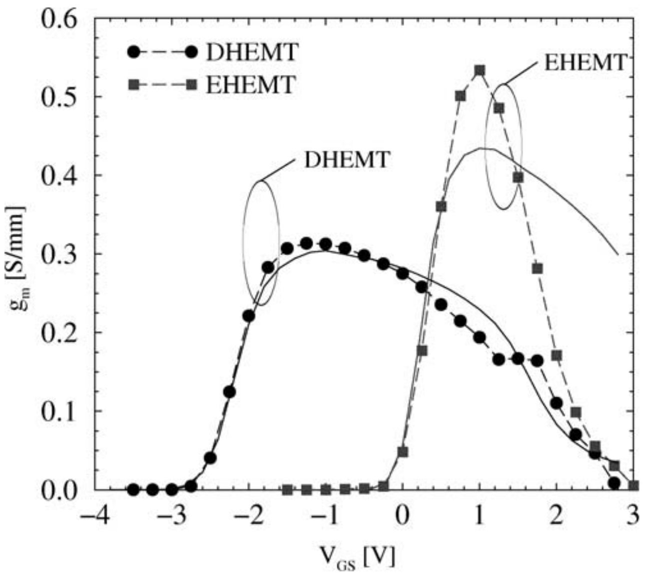

Figure 3. Transconductance at V_{DS}=7 V: lines – simulation, symbols – experimental data

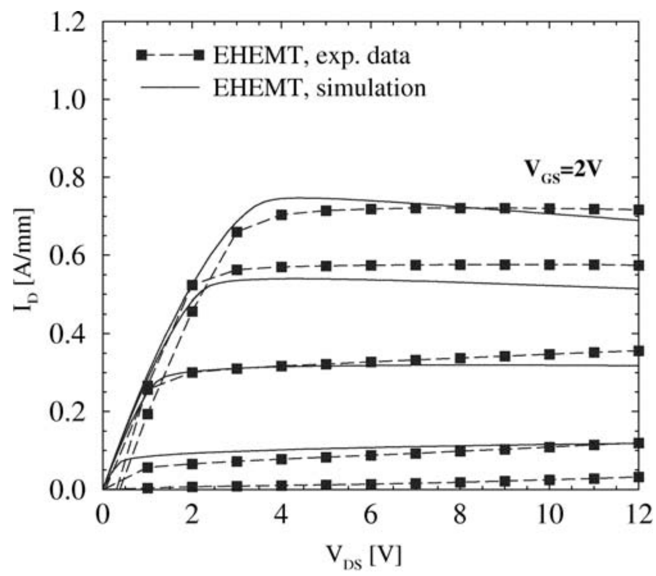

Figure 5. Comparison of the output characteristics (EHEMT), V_{GS} stepping 0.5 V

IV. Simulation Results

Fig. 2 compares the simulated transfer characteristics to experimental data. Both devices are simulated using the same set of models and model parameters, including the interface charge densities. A good agreement is obtained, both for the threshold voltage and the transconductance g_m (Fig. 3). A possible explanation for the underestimation of the peak g_m for the recessed device is an overestimation of the sheet resistance under the gate. Simulated output characteristics for both structures are compared to continuous wave (CW) measurements in Fig. 4 and Fig. 5.

The RF simulations provide slightly higher cut-off frequency than the experiments for both structures (Fig. 6). Note, that both the measured and simulation data show an increase of the cut-off frequency f_T and the maximum frequency f_{max} for the EHEMT structures.

Since the gate capacitance depends on the gate – channel distance, we perform several simulations with variable recess depth, i.e. variable barrier thickness t_{bar} under the gate. As expected a shift in the threshold voltage is observed (Fig. 7), and g_m increases with decreasing t_{bar} (Fig. 8) due to the lack of charge control for thicker layers.

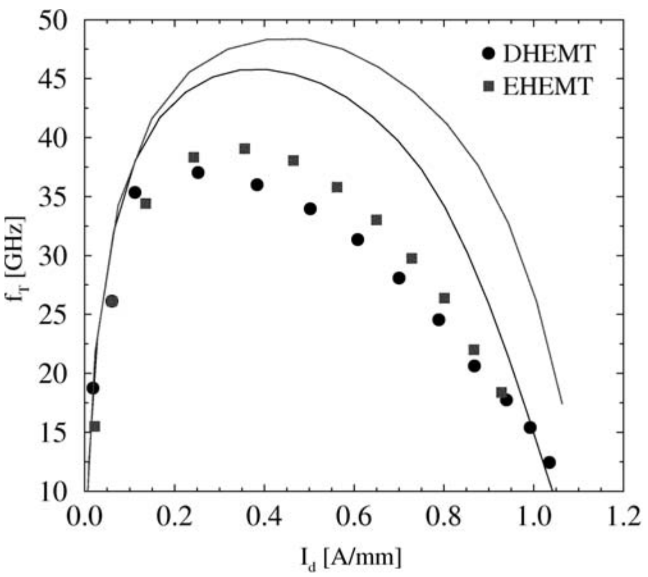

Figure 6. Comparison of the cut-off frequency f_T: symbols - simulation, lines - experimental data

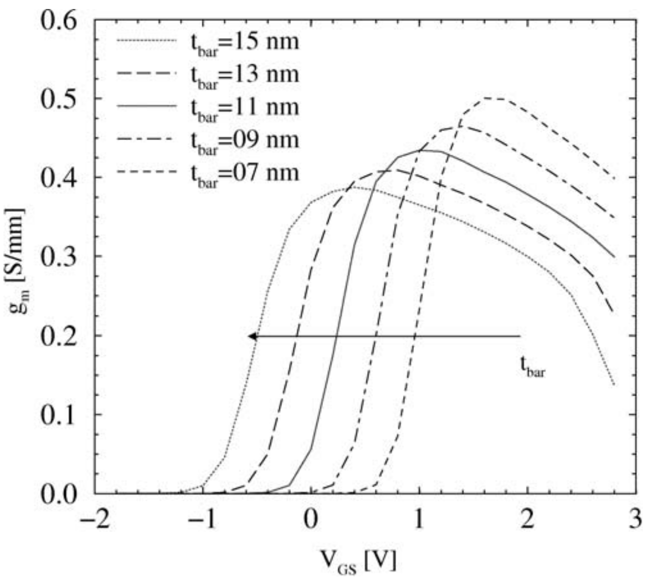

Figure 8. Simulated transconductance for devices with different barrier thickness t_{bar} under the gate

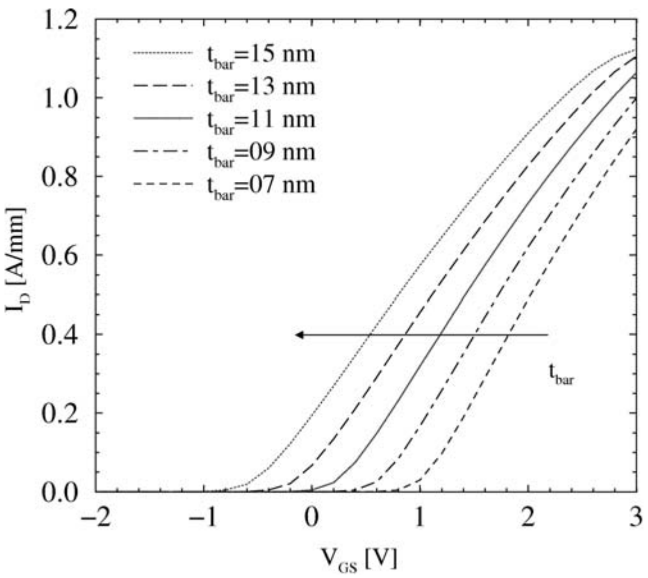

Figure 7. Simulated transfer characteristics for devices with different barrier thickness t_{bar} under the gate

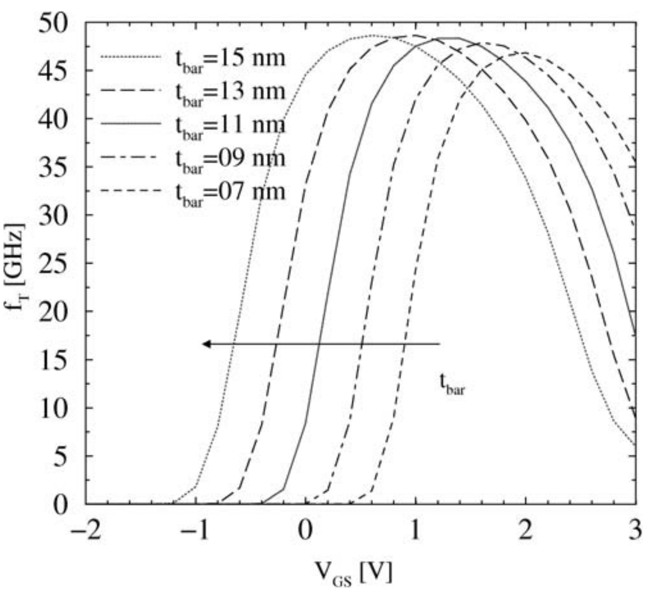

Figure 9. Simulated cut-off frequency for devices with different barrier thickness t_{bar} under the gate

However, the simulated f_T characteristics show no noticeable change (Fig. 9). Fig. 10 shows the gate-source capacitance. It increases with decreasing t_{bar}, so it compensates the increase in g_m, thereby resulting in a constant f_T. Thus, the major reason for the rise of f_T and f_{max} of the EHEMTs in comparison to DHEMTs (Fig. 4) is the absence of barrier/cap negative interface charges under the gate. The exact depth of the recess has less influence on f_T and f_{max}, but it has significant impact on the threshold voltage and the transconductance.

V. Conclusion

In this work we study the DC and RF performance of AlGaN/GaN HEMTs with recessed gates. Our device simulator is calibrated against measured data and used subsequently for the exploration of the impact of the gate recess depth. Our results show, that while the exact recess depth has a major impact on the threshold voltage and transconductance, the cut-off frequency of the EHEMTs remains relatively unchanged due to the increase of the gate-source capacitance.

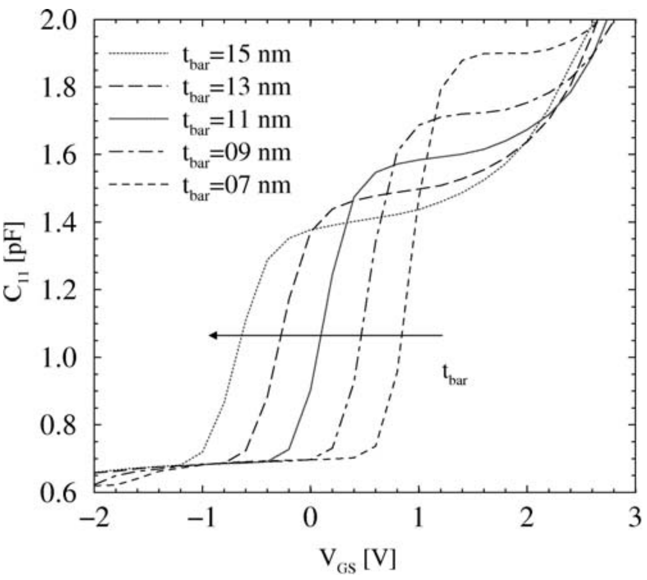

Figure 10. Simulated gate-source capacitance for devices with different barrier thickness t_{bar} under the gate

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